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FPGA Implementation of Optimized CIC Filter for Sample Rate Conversion in Software Radio Receiver

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***Abstract*— A software radio receiver is one which is tuned to receive a transmitted signal on multiple communication standards through software rather than hardware. To incorporate multi-standard radio communications an intermediate frequency of high ranges is used. Such high intermediate frequencies when sampled with Nyquist rate gets oversampled due to the phenomenon of Band Pass sampling depending on the radio communication standard. Hence a digital down converter (DDC) capable of reducing the sampling rate in accordance with the radio communication standard is required. Cascaded Integrated Comb (CIC) filters are used for large sample rate conversion factors. In this paper an optimized architecture for DDC employing CORDIC in the mixer stage and the reconfigurable decimation factors for CIC filters has been implemented. Optimized implementation of CIC filter for sample rate conversion of multi-standard radio communications reduces the hardware resources by more than twenty percent when compared with the non-optimized architecture.**

***Index Terms*— DDC, CORDIC, FPGAs, CIC Filter, SRC.**

I. Introduction

An ideal software radio receiver needs an analog to digital converter to be placed as close as possible towards the antenna. As the signal at the antenna is in radio frequency ranges, positioning ADC at this stage poses high sampling rate requirements leading to very high power dissipation. Hence the existence of an ideal software radio is impractical. Therefore the radio receiver is broadly divided into three stages. Firstly, Radio Frequency stage, where the incoming radio frequency signals is heterodyned with local analog oscillator such that a high intermediate frequency signal comprising of multiple radio communications standards is generated. Secondly, intermediate frequency stage where digitization, sample rate conversion and channelization are the three tasks carried out. Thirdly, baseband stage where the baseband signal processing such as filtering, demodulation, decoding are carried out [1].

The focus of this work is in the IF stage of the radio receiver. The intermediate frequency of signal in the IF stage is of the order of few tens of Mega Hertz. The process of sample rate conversion and channelization are highly computationally intensive tasks. An illustration of sample rate conversion and channelization shows that the process requires two high end Digital signal processors per channel which is cost ineffective solution. Therefore, reconfigurable FPGAs provide high design flexibility which offers high speed and a reconfigurable solution [2].

An architecture for implementation of mixer and CIC filter for down conversion of an intermediate frequency signal to a baseband signal of single GSM 900 standard is proposed and the estimate of hardware resource utilization is provided [7]. As the software radio receiver needs to adapt the multi-standard radio communication standards, a down converter capable of down conversion of GSM900, WCDMA, CDMA2000 and HiperLAN 802.16 is implemented based on the method of factorization and a hardware resource estimate is made which is not taken into account by Sheikh Et.al [1]. CIC filters are optimized to reduce area and power requirements and the reduction in the hardware resource requirements is estimated through a mathematical formula.

In this paper prototype architecture for down conversion of IF signal with reconfigurable sample rate change factors has been implemented. The IF frequency is chosen to be 80MHz and this signal is down converted using three stage CIC filters with variable decimation factors of 2,4,6 and 8 in each stage. The architecture implemented can down convert with decimation factors ranging from 2 to 512. For decimation factor greater than eight the decimation factors for CIC filters are provided in such a way that the power is optimized. The pipelined architecture is simulated with XC6VCX75t-2FF484 VIRTEX-6 device, operating at a maximum operating frequency of 240MHz. An attempt has been made to estimate the hardware resource utilization of this DDC on FPGA and compare with optimized sample converter for four standards.

This paper is organized as follows. Section II describes the theory of DDC, CORDIC algorithm, digital filters and illustrative specifications of different wireless standards. Section III presents the calculations for realization of multi-mode, multi-standard software radio and the implemented architecture for DDC. Section IV presents the results with a simulation setup on Virtex-6 XC6VCX75t-2FF484 FPGA and conclusions are presented in section V.

II. Theory

A. Digital down converter

The basic architecture of a digital down converter as shown in figure 1 employs a Numerically Controlled Oscillators (NCO), mixers, decimator and filters as its building blocks. The digitized incoming IF signal is heterodyned with NCOs

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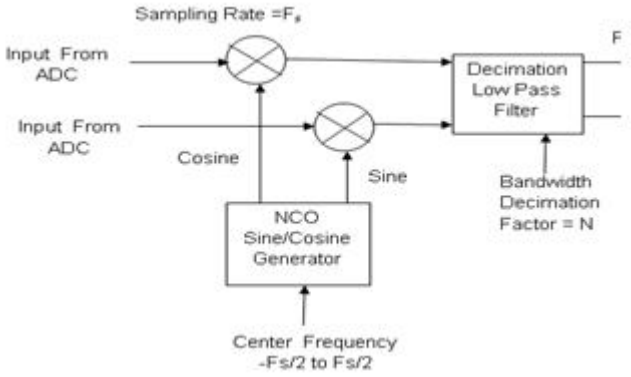

Figure 1 Block diagram of a Digital Down converter

in quadrature which produces the sum and difference components of in phase and quadrature channels respectively. Equation 1 shows the frequency translation of the mixed signal. The sum component is a high frequency component which is eliminated and the baseband difference component is passed through a decimation filter and then sampling rate is converted.

$$cos\omega_c t\ x(t) \leftrightarrow 0.5[X(\omega-\omega_c)+X(\omega+\omega_c)]$$
$$sin\omega_c t\ x(t) \leftrightarrow j0.5[X(\omega-\omega_c)+X(\omega+\omega_c)] \quad (1)$$

where, x(t) is the input signal, X(ω) is its Fourier transform and ω_c is the carrier frequency of the signal.

B. CORDIC Algorithm

CORDIC is an acronym for COordinate Rotation DIgital Computer. CORDIC algorithm is developed based on Given's Rotation and it is first used for computation of trigonometric functions employing shift and add operations [3]. Later the use of CORDIC has been extended for computation of multiplication, division, exponential functions, and logarithmic functions, rectangular to polar conversion as generalized by J.S.Walther [4]. The iterative equations of radix-2 CORDIC algorithm for vector rotation of coordinates in Cartesian coordinate system are given as

$$x_{i+1} = x_i - \sigma_i y_i 2^{-i}$$
$$y_{i+1} = y_i + \sigma_i x_i 2^{-i}$$
$$z_{i+1} = z_i - tan^{-1}(\sigma_i 2^{-i}) \quad (2)$$

where, σ_i represents the direction of rotation in each iteration and arcTan (2^{-i}) is an elementary rotation angle. As the CORDIC rotation results in a constant gain (K), the magnitude of the vector increases. The norm of the vector is preserved by scaling the final coordinates by K^{-1}, the CORDIC scale factor

$$K^{-1} = \prod_{i=1}^{n} \sqrt{1+\sigma_i{}^2 2^{-2i}} \quad (3)$$

For a CORDIC architecture implemented in radix-2 number system, scale factor compensation can be achieved through constant canonical signed digit multipliers. We have employed CORDIC Algorithm for the design of a numerically control oscillator and a mixer in communication system receiver design. The advantage of using CORDIC algorithm is it eliminates the need of phase shifter and thereby reducing phase distortions and also explicit multipliers are eliminated thus a great reduction in the hardware resources when compared with the conventional Look Up table approach [5] [6].

C. Digital Filters

The aliasing components generated due to decimation has to be suppressed and hence digital filters are employed. Multi-rate signal processing involves low pass filter as its fundamental block. A low pass filter implemented with normal multiply and accumulate operation requires high speed multipliers operating at a frequency of twice the intermediate frequency leading to high power dissipation. Thus Hogenaeur proposed a special class of filters called Cascaded Integrator Comb filters which are used for removing aliasing components when the decimation rates are high[9]. Due to multiplier less architectures of CIC filters the process of sampling rate conversion is highly aided. In a CIC filter of order N, N integrators operate at high frequency and N combs operate at low frequency. Equation 7 shows the transfer function of CIC filter. Though CIC filters are simple in design their bit growth requirements make them high instable. CIC filters suffer from the disadvantage that it has a large droop in the required pass band. However this droop can be restored by employing a droop compensation filter operating at a frequency of the baseband signal.

$$H(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} \quad (4)$$

Where R = Decimation Factor, M = Differential delay (1 or 2), N = No of Integrators/Combs.

D. Specifications

The intermediate frequency of signal for Mobile communications is taken as 80MHz. This signal is digitized with high speed analog to digital converters with a Nyquist sampling rate and has to be passed through a DDC to extract the baseband signal at a required sampling rate. Table I shows the specifications for multi-mode multi-standard radio communication systems with four popular standards, which is extended for decimation with variable decimation factors.

III. Architecture

In order to address the problems related to the phase distortions due to phase synchronization and errors due to mixing operations, CORDIC algorithm is used to generate quadrature waveforms and multiplier less mixing operation. CORDIC based DDCs have good SFDR when compared with the conventional Look up table approach [8]. As per the taxonomy of CORDIC architectures there are various implementations of CORDIC algorithm. Based on the number system employed it can be implemented using radix-2, radix-4 and so on. While the radix-2 CORDIC architecture has constant scale factor the other number systems employs a separate unit for the computation of scale factor. Higher radix CORDIC architectures have low latency as the number of iteration stages can be reduced at the cost of more hardware. Based on the architecture CORDIC algorithm can be implemented using

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TABLE I. SPECIFICATIONS FOR MULTI-STANDARD SOFTWARE RADIO

Radio Standard	WiMAX 802.16	WCDMA (UMTS)	CDMA (IS-95)	GSM 900
Intermediate Frequency(MHz)	80	80	80	80
Sampling Rate(MSps)	160	160	160	160
Single Channel Bandwidth(MHz)	20	5	1.25	0.2
Required Sampling Rate(MSps)	40	10	2.5	0.4
Over sampling Ratio	4	16	64	400
Target Data Rate(Mbps)	10	3.84	1.2288	0.270
Sample Rate Conversion Ratio	1/8	6/125	48/3125	677/200000

redundant adders and non-redundant adder architectures. Redundant adder when employed reduces the stage delay and has high throughput due to non-propagation of the carry whereas doubles the required hardware when compared with non-redundant architecture [6].

As per the specifications the intermediate frequency of the signal of radio receiver is 80MHz. As per Nyquist criterion we need a CORDIC architecture whose throughput is 160MSps. CORDIC architecture using redundant carry save adders and non-redundant carry look-ahead adders are implemented in this work. In non-redundant carry look-ahead architecture we have obtained a throughput of 240MSps which is well within the required throughput. Non-redundant CORDIC architecture is employed not only to reduce the area within the CORDIC cell itself but also to reduce the area in the subsequent stages of the system design. The pipelined CORDIC architecture is implemented with 16-bit precision using carry look-ahead adders and CIC filters are implemented on Virtex-6 XC6VCX75t-2FF484 device.

A. Numerically Controlled Oscillator

The structure of a numerically controlled oscillator consists of two blocks viz, phase accumulator and phase to amplitude (sine/cosine) generator. The digital output of the phase to amplitude generator is fed to Digital to Analog Converter and then passed through a low pass filter to remove the unwanted frequency components. The frequency of the NCO is controlled by the frequency control word f_{cw}, which is nothing but the phase increment given to the phase accumulator. In each clock cycle the phase accumulator increments itself by that value until it overflows and wraps around. Thus the frequency of NCO is given by

$$f_c = F_{clk} * \frac{f_{cw}}{2^{n-1}} \tag{5}$$

Where, F_{olk} = Frequency of the clock, f_{ace} = Required local oscillator frequency and f_{ew} =Frequency control word. The frequency control word has been configured such that the numerically controlled oscillator frequency is tuned to 80MHz.

B. Digital Down Converter Block

As stated earlier, Equation (1) describes the rotation of the vectors by an angle θ. The CORDIC module is configured in the circular rotation mode with inputs being $x_0 = x_{if} \cos(\omega_{if} n)$, $y_0 = 0$, $z_0 = \omega_c n$ as shown in figure. The output of the CORDIC module is given by the equation (6), generating the in phase and quadrature phase mixer outputs.

$$\begin{aligned} x_{out} &= K^{-1} x_{if} cos(\omega_{if} n) cos(\omega_c n) \\ y_{out} &= K^{-1} x_{if} cos(\omega_{if} n) sin(\omega_c n) \\ z_{out} &= 0 \end{aligned} \tag{6}$$

According to the trigonometric identities, the output of the CORDIC module has two frequency components viz, $\omega_{if} + \omega_c$ and $\omega_{if} - \omega_c$. The frequency components $\omega_{if} = \omega_m + \omega_c$, ω_c = 80MHz to generate a difference component of ω_m with 160MS/s, which has to be decimated by a decimation factor are chosen as shown in table I for Nyquist sampling rate.

C. Filtering And Decimation

The process of decimation employs a low pass filter along with a decimator. As the incoming signal is at a very high sampling rate, high speed multipliers are needed to implement the MAC operations in low pass filters. An alternate is employing a multiplier less filter architecture at high sampling rate and conventional MAC operations at lower sampling rate. Multiplier less CIC filter architecture is the best choice to down convert a signal when high decimation rate is required and a narrow band signal has to be extracted from a wide band signal [9].

A pipelined architecture has been implemented for CIC filters in three stages using three integrators and three differentiators. Table II shows the decimation factors as calculated by the factorization method stated by Sheikh Et.al [1]. The CIC filter architecture has been extended such that CIC filter can take any one of the decimation factors among 2, 4, 6 and 8. In order to optimize power the decimation factors for the CIC filters are provided in such a way that the mixer output is decimated with the highest possible decimation factor at the earlier stage of the CIC filter and lower decimation factors in the subsequent stages of the filter. For example to decimate a signal with decimation factor of 96 the possible factors of decimation for CIC1, CIC2 and CIC3 are 8, 6 and 2 respectively. Table III shows the calculation of various decimation factors for the three stages of implemented CIC filter. We have optimized the architecture of CIC by reducing the number of bits within a particular CIC stage and from one stage to another by normalizing the gain of filter to unity. The total bit growth of the filter is given by equation 7.

$$B_{Total} = N * log_2 R + B_{in} \tag{7}$$

where B_{Total}: the total number of bits required, N: Order of the CIC filter, R: Required Decimation rate, B_{in}: Input width of the data.

As the order of the CIC filter increases the bit growth requirements for implementation of CIC filter also increases leading to high utilization of hardware resources. To illus

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trate a CIC filter when implemented with R=384, N=9 and 16-bit precision leads to a bit growth of 97 bits. On the other hand cascade implementation of CIC filters in three stages with N=3 each require 43 bits at its input [9].

TABLE II. DECIMATION FACTOR OF CIC FILTERS FOR MULTI-STANDARD RADIO

Standard	OSR	CIC 1	CIC 2	CIC 3
WiMAX	4	4	1	1
WCDMA	16	8	2	1
CDMA2000	64	8	8	1
GSM	400	8	8	6

TABLE III. POSSIBLE DECIMATION FACTOR FOR CIC FILTERS

Overall Decimation Factor	CIC I	CIC II	CIC III
2	2	1	1
4	4	1	1
6,12,24,36	6	1,2,4,6	1
72,144,216	6	6	2,4,6
8,16,32,48,64	8	1,2,4,6,8	1
96,192,288	8	6	2,4,6
128,256,384,512	8	8	2,4,6,8

To further optimize the hardware resources the gain of the CIC filter is normalized to unity. The gain of the filter in each stage is given as

$$G_{CIC} = (R_i)^{N_i} \tag{8}$$

To minimize the hardware resources within the stage itself, the output at each integrator is arithmetic right shifted by $\log_2(R_i)$ bits normalizing the gain of the filter to unity. Figure 2 shows the gain normalized in the stage 1 which can be extended to the other stages of the CIC filter. Figure 3 shows the implementation of a multistage CIC filter with optimized number of bits. Equation 9 shows the number of bits reduced and the number of adders optimized per CIC stage respectively.

$$B_{i,opt} = N_i * log_2(R_i)$$

$$\begin{aligned} A_{i,opt} =& log_2(R_i) + 2 * log_2(R_i) + ... \\ & ..... + N_i * [N_i * log_2(R_i)] \end{aligned} \tag{9}$$

Where, $B_{i,opt}$ Number of bits optimized in each integrator stage, $A_{i,opt}$: Number of adders optimized in i^{th} stage, R_i: Decimation factor in i^{th} stage, N_i: Order of i^{th} stage CIC filter.

A filter architecture when implemented using p stages with filter order $N=\sum_{i=1}^{p} N_i$ and the required decimation factor $R=\prod_{i=1}^{p} R_i$ the total number of adders that can be optimized is given by equation (10).

$$\begin{aligned} A_{opt} =& \sum_{i=1}^{P} [log_2 R_i [\frac{1}{2}(3N_i^2 - N_i)] \\ & + (2N_i) \sum_{j=0}^{i-1} N_j log_2 R_j] \end{aligned} \tag{10}$$

where A_{opt} represents the total number of adders optimized and P: Number of CIC stages.

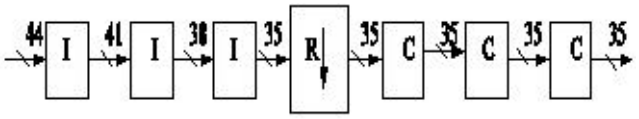

Figure 2 Architecture of Stage 1 CIC filter

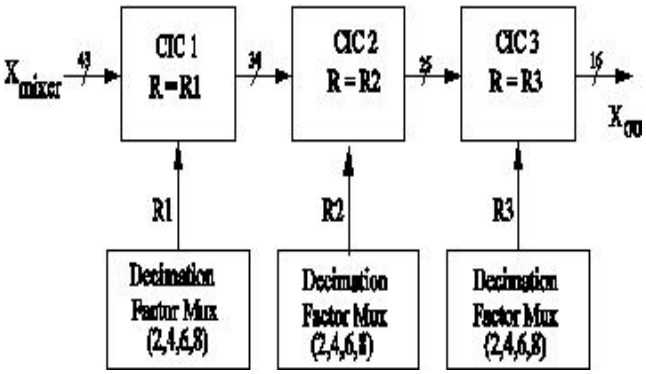

Figure 3 Architecture of Multi-Stage CIC filter

RESULTS

The simulation setup for testing prototype DDC shown in figure 4 uses CORDIC based digital synthesizers/mixers to generate a baseband signal of low frequency, frequency modulated wave with a carrier frequency of 80MHz and demodulated. CIC filters as stated in section 3.3 are implemented to extract the inphase and quadrature component of the baseband signal at a lower sampling rate. The design is implemented on VIRTEX-6 XC6VCX75t-2FF484 FPGA and the simulation results are shown in figures [5-7]. In the present work, CIC filters have reconfigurable decimation factors rather than the fixed decimation factor. The decimation factor for CIC filter is reconfigured based on the required rate change. As the decimation factors in the CIC stages are reconfigured the number of stages of CIC filters has been reduced from four to three in comparison to the Sheikh's architecture thereby saving hardware resources [1].

Device utilization summary for Digital down conversion of the in-phase and the quadrature channel for a multi-channel radio with an area optimized reconfigurable decimation rate and an optimized sample rate converter with fixed decimation factors in each stage of CIC filter is tabulated in table IV and the comparison shows twenty percent savings in the hardware resources.

TABLE IV. HARDWARE RESOURCE UTILIZATION ON XC6VCX75T-2FF484 FPGA

Hardware Resources	Fixed Factor	Arbitrary Factor
No. of Slice Registers	3337	2109
No. of Slice LUTs	5898	4793
No. of Slice LUT-FF Pairs	2486	1620
Frequency(MHz)	355	355

For simulation a baseband sinusoidal signal with 128 samples is generated by configuring the frequency control word of the phase accumulator of the first CORDIC cell which generates a frequency of 312 KHz. These samples are fre

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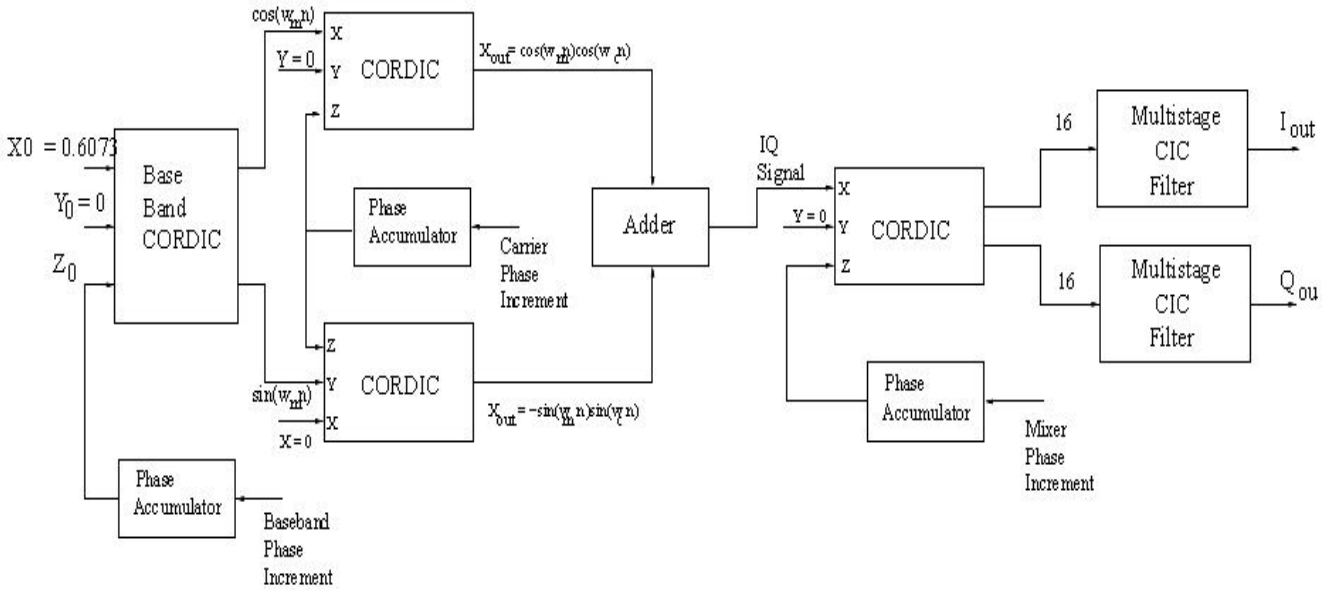

Figure 4 Simulation Set up of CORDIC based DDC

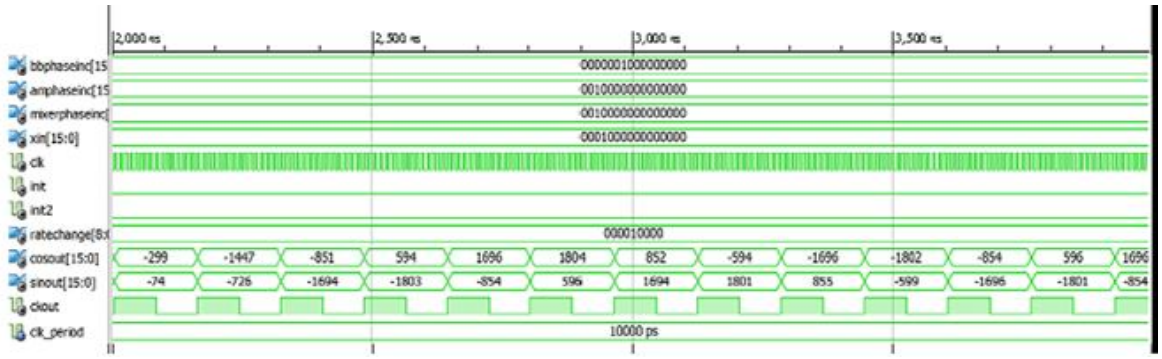

Figure 5 Simulation Result of Sample Rate Conversion with Decimation factor =16

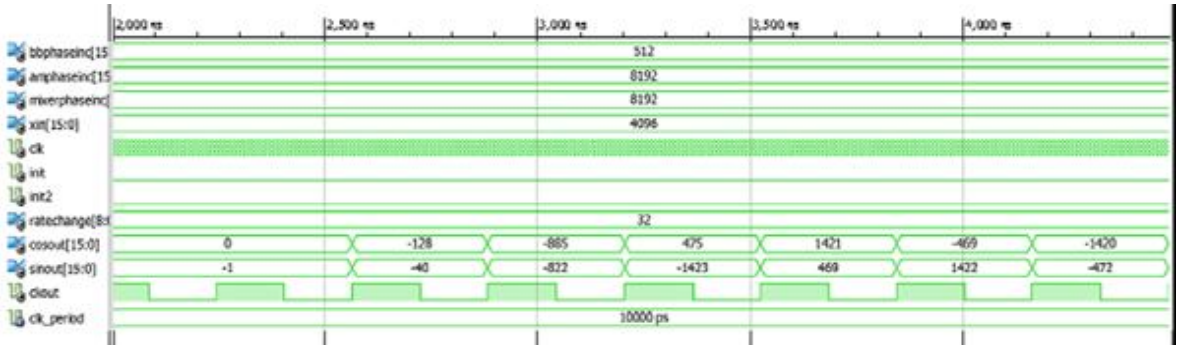

Figure 6 Simulation Result of Sample Rate Conversion with Decimation factor =32

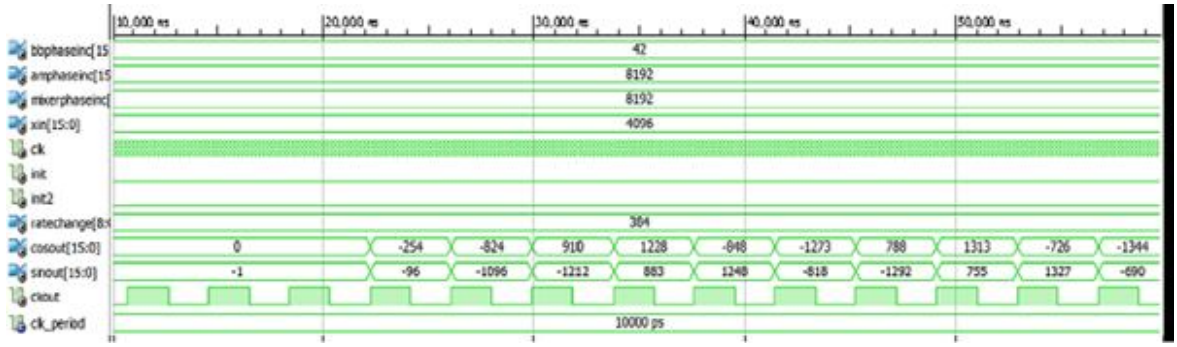

Figure 7 Simulation Result of Sample Rate Conversion with Decimation factor =384

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quency modulated and demodulated with a carrier frequency of 80MHz. The demodulated signal has been decimated with a decimation factor of 16 and 32 and found that the number of samples in the baseband signal is eight and four respectively as shown in figures 5 and 6. As per the GSM 900 standard the required decimation factor is 384. The frequency control word of the CORDIC module was configured such that 1536 samples of the baseband are generated. Figure 7 shows after demodulation and decimation the number of samples is found to be four for GSM900 standard and thereafter sample repetition occurs.

Conclusions

Area optimized architecture has been simulated for arbitrary sample rate conversion for a software radio receiver on Virtex-6 XC6VCX75t-2FF484 FPGA based on the method of factorization of decimation rates. As the numerically controlled oscillator and quadrature mixer is implemented using CORDIC architecture hardware resources are optimized due to elimination of Look Up tables and phase shifters. CORDIC based NCOs have a high SFDR due to elimination of errors like phase to phase mapping, phase truncation and phase synchronization errors. As the CIC filter in former stage is subjected to high decimation factor the subsequent stage of CIC filters operates at a lower frequency hence power dissipation is also reduced to a great extent. Further a programmable interpolation and sample rate conversion filter to match the symbol rate of the standard has to be implemented on FPGA.

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